FIG. 1

SOURCE CODE — 8

↓

COMPILER/ASSEMBLER — 9

↓

EXECUTABLE CODE — 10

LC   LC   LC   16

HOST SYSTEM

12-F

EMULATOR$_2$ — 12-2

EMULATOR$_F$

TC$_2$ TC$_F$

13-1   14-1   13-2   13-F
                           14-2   14-F

OPERATING SYSTEM$_1$ OPERATING SYSTEM$_2$ ● ● ●   OPERATING SYSTEM$_F$

HARDWARE SYSTEM$_1$ HARDWARE SYSTEM$_2$ 15-F   HARDWARE SYSTEM$_F$

15-1   15-2

FIG. 2

16

26   HOST SYSTEM

PROGRAM EXECUTION INFORMATION

LC

GROUP ACCESS   LC$_G$ LEGACY CODE TRANSLATOR   TRANSLATOR STORE — 24

10   21

13-F

EXECUTION UNIT   TC$_F$ TRANSLATED CODE CACHE

23

Atty: David E. Lovejoy
Tel No: 415-362-3800

Atty Doc No: AMDH-08157US0 DEL
Inventor 1: Ronald Hilton

Express Mail No:
EL622696054US

Title: STATE-SPECEFIC VARIANTS OF TRANSLATED CODE UNDER EMULATION

2/3

LEGACY CODE (CISC)

```
100   START   BALR   B1,R0
102   BASE    LM     R1,R2,DATA1
106           MVC    DATA1, DATA3
10C           A      R1,DATA2
              H
110           SRA    R1,1
114           SH     R2,DATA2
118           AR     R1,R2
11A           BC     TARGET
120   DATA1   DC     X'005390BC'
              DC     X'09C20004'
128   DATA2   DC     X'0009'
12A   DATA3   DC     X'800039AF'
```
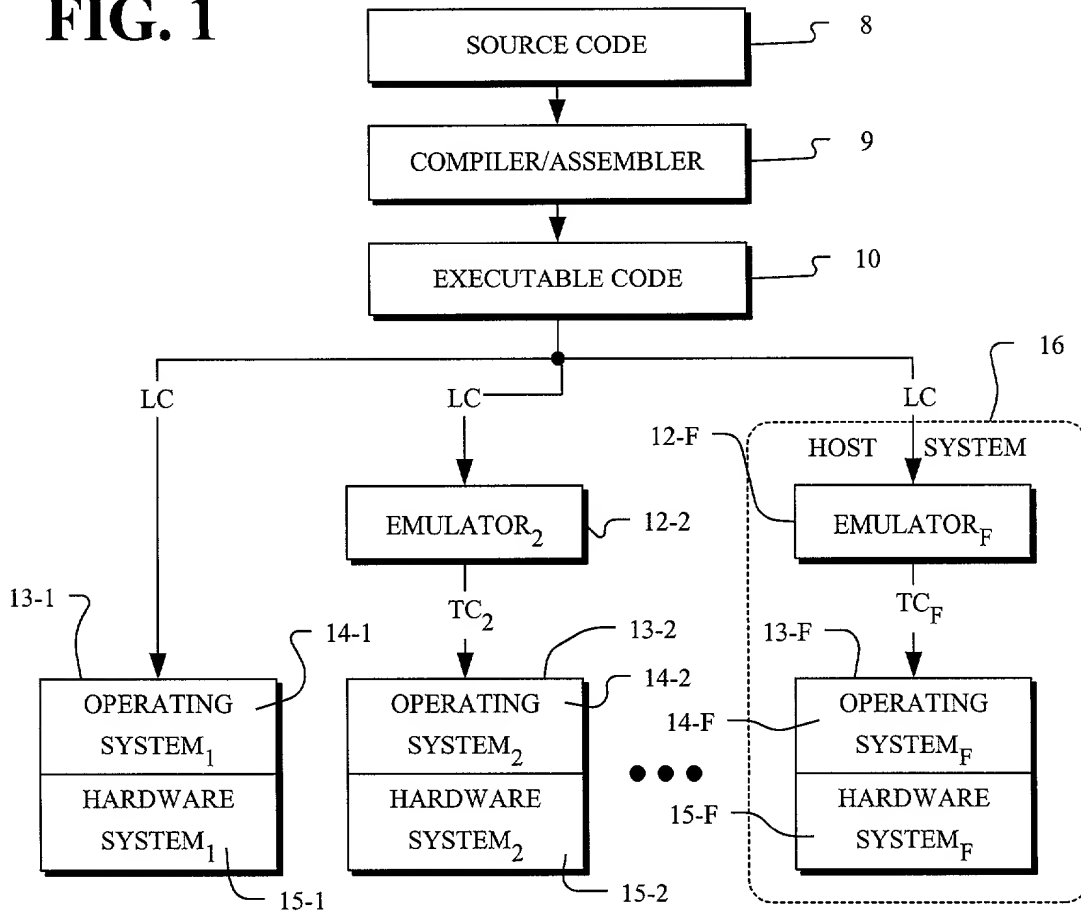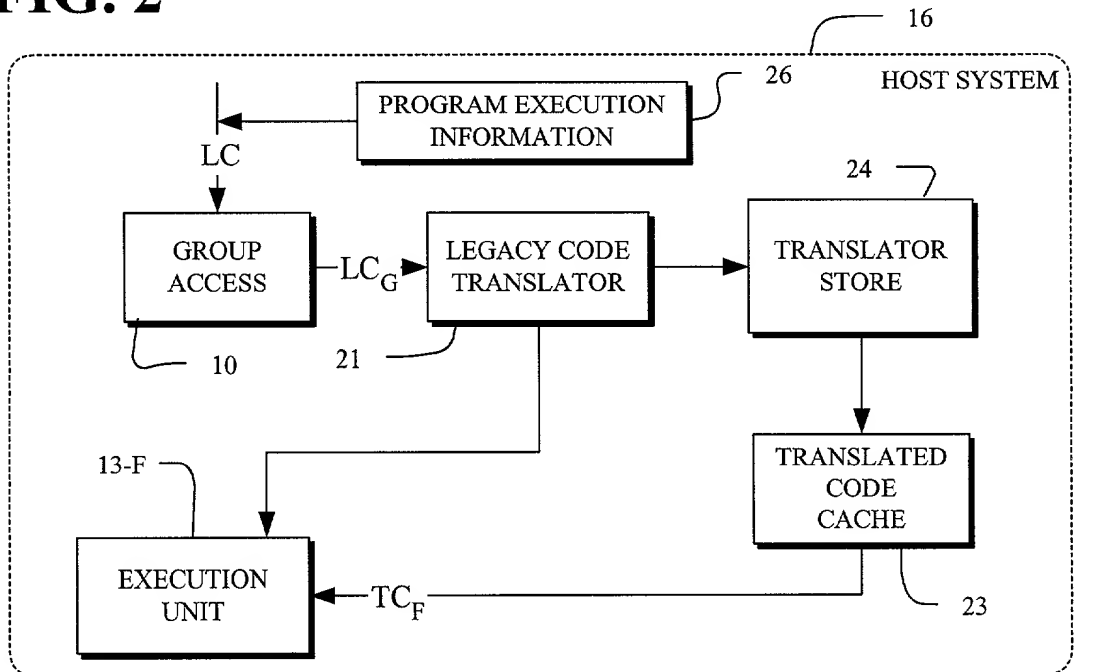
FIG. 3

```
100   START   BALR   B1, R0
102   BASE    LM     R1, R2,DATA1
106           MVC    DATA1, DATA3
10C           A      R1, DATA2
              H
```

3_C-10

3_R-10

TRANSLATED CODE (RISC)

```
BALR  MOV  B1   BASE
LM    AD   A1   B1,DATA1- BASE
      LD4  R1   [A1]
      AD   A1   A1,4
      LD4  R2   [A1]
MVC   AD   A1   B1,DATA1-BASE
      AD   A2   B1,DATA3-BASE
      LD4  T1   [A2]
      ST4  T1   [A1]
A     AD   A1   B1,DATA2 -BASE
      LD2  T1   [A1]
H     AD   R1   R1,T1
      B    XFER_SEQUENTIAL
```

3_C-11

3_R-11

```
110           SRA    R1,1
114           SH     R2,DATA2
118           AR     R1,R2
11A           BC     TARGET
```

```
120   DATA1   DC     X'005390BC'
              DC     X'09C20004'
128   DATA2   DC     X'0009'
12A   DATA3   DC     X'800039AF'
```

3_C-12

```
SRA   SHR  R1   1
SH    AD   A1   B1,DATA2 -BASE
      LD2  T1   [A1]
      SUB  R2   R2,T1
AR    AD   R1   R1,R2
BC    AD   A1   B1,TARGET - BASE
      B    XFER_BRANCH
```

Current Date:14/11/01   Time Edit:14/11/01-12:17   Time Print:14/11/01-12:18
Path:m:\del\wp\amdh_all\amdh8\8157pa\dwg\
Name:8157_01^11^14-fi.vsd

Atty: David E. Lovejoy
Tel No: 415-362-3800

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3/3

FIG. 4

LEGACY CODE (CISC)

STATE = 0000000000004200

3_S

0F0	TM	PERFLAG
0F4	BNE	START
0F8	SSM	ENBLPER
0FC	LCTL	CR9,STOREPER

3_C-0F

3_R-10'

TRANSLATED CODE (RISC)

0000000000000000 (PER OFF)

100	START	BALR	B1, R0
102	BASE	LM	R1, R2,DATA1
106		MVC	DATA1, DATA3
10C		A H	R1, DATA2

3_C-10

3_R-10

0000000000004200 (PER ON)

BALR	MOV	B1	BASE
LM	AD	A1	B1,DATA1- BASE
	LD4	R1	[A1]
	AD	A1	A1,4
	LD4	R2	[A1]
MVC	AD	A1	B1,DATA1-BASE
	AD	A2	B1,DATA3-BASE
	LD4	T1	[A2]
	ST4	T1	[A1]
	CMP	A1, C10
	BLT	AH
	CMP	A1, C11
	BGT	AH
A	B	PER_RUPT
	AD	A1	B1,DATA2 -BASE
H	LD2	T1	[A1]
	AD	R1	R1,T1
	B	XFER_SEQUENTIAL

3_C-11

3_R-11'

3_R-11

110		SRA	R1,1
114		SH	R2,DATA2
118		AR	R1,R2
11A		BC	TARGET

120	DATA1	DC	X'005390BC'
		DC	X'09C20004'
128	DATA2	DC	X'0009'
12A	DATA3	DC	X'800039AF'

3_C-12

0000000000000000 (PER OFF)

0000000000004200 (PER ON)

SRA	SHR	R1	1
SH	AD	A1	B1,DATA2 -BASE
	LD2	T1	[A1]
	SUB	R2	R2,T1
AR	AD	R1	R1,R2
BC	AD	A1	B1,TARGET- BASE
	B	XFER_BRANCH

Current Date:14/11/01   Time Edit:14/11/01-12:17   Time Print:14/11/01-12:18
Path:m:\del\wp\amdh_all\amdh8\8157pa\dwg\
Name:8157_01^11^14-fi.vsd